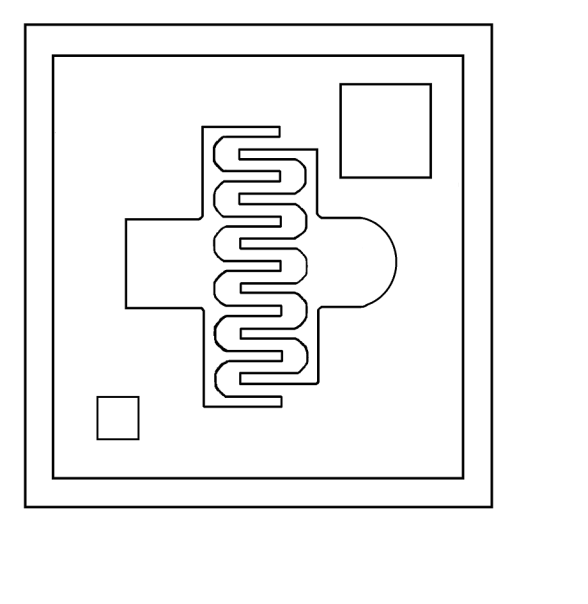
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**S**

**D**

**.017”**

**.017”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” min.**

**Backside Potential: Gate**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .017” X .017” DATE: 10/20/21**

**MFG: INTERSIL THICKNESS .008” P/N: 2N4416**

**DG 10.1.2**

#### Rev B, 7/19/02